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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,483	01/17/2002	Yangsung Joo	501087.01	1430

7590 05/27/2005

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/051,483	Applicant(s) JOO ET AL.	
	Examiner Jason M. Perilla	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-74* is/are pending in the application.

4a) Of the above claim(s) *12-19,32-39 and 66-74* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-47 and 57-62* is/are rejected.

7)☒ Claim(s) *1-11,20-31,40-43,48-56 and 63-65* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/17/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-74 are pending in the instant application.

Election/Restrictions

2. This application contains claims directed to the following patentably distinct embodiments of the claimed invention:

I. Claims 1-65, drawn to a data output circuit, classified in class 375, subclass 354.

II. Claims 66-74, drawn to a data output circuit, classified in class 375, subclass 354.

3. Inventions I and II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions are not capable of use together and have a different mode of operation and different effects. In embodiment I of figure 3, each data driver (DQ1-DQN) receives the same phase shift clock signal (CLKDEL). However, in embodiment II of figure 8, each data driver (DQ1-DQN) receives a respective phase shift clock signal (DC1-DCN). This variation in phase shift clock signal application among the data drivers leads to different modes of operation and different effects between the embodiments I and II.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. This application contains claims directed to the following patentably distinct species of the first embodiment (embodiment I; claims 1-65 – above) of the claimed invention:

Species i; Claims 6-11 and 27-31, Figure 5.

Species ii; Claims 12-15 and 32-35, Figure 6.

Species iii; Claims 16-19 and 36-39, Figure 7.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claims 1-5, and 25-26 are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the

case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

6. During a telephone conversation with Kimton Eng (43605) on May 18, 2005 a provisional election was made without traverse to prosecute the invention of the first species i of embodiment I, claims 1-11, 20-31, and 40-65. Affirmation of this election must be made by applicant in replying to this Office action. Claims 12-19, 32-39, and 66-74 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 60 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 60, the specification does not enable one to utilize three data signals in a group for comparing current and future logic states. That is, every species of the first embodiment of the invention utilizes only two signals: the future and current (figs. 5-7; DQ0, RD0).

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 44-47 and 57-62 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

Regarding claim 44, the omitted steps are (line 7): adjusting the delay interval in response to the determined output delay.

Regarding claims 45-47, the claims are rejected as being based upon a rejected parent claim.

Regarding claim 57, the omitted steps are (line 7): outputting the data signal having the second logic state in response to the output delay.

Regarding claims 58-62, the claims are rejected as being based upon a rejected parent claim.

11. Claims 51-56, 59 and 64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 51, the claim is indefinite because one is unable to determine the number of logic signals claimed. The preamble defines "data signals", and current and future logic states *of the data signals* are further defined. However, "each data signal having the current logic state" (lines 3-4) and "each data signal having the future logic state" (lines 7-8) are further defined (without having definite antecedent basis). Therefore, one is unable to determine definitively the number and type of data signals

being claimed because data signals having the future logic state and data signals having the current logic state are exclusive although not definitely claimed.

Regarding claims 52-56, the claims are rejected as being based upon a rejected parent claim.

Regarding claim 59, the claim is indefinite because "a group of data signals" and "the data signals" becomes confused in the claim. In line 4, "a group of data signals" is associated with "(a one of) the data signal(s)", however, in lines 6-7, "the data signals in the group" is stated (having no definite antecedent basis). Therefore, one skilled in the art is unable to definitively determine if the group of data signals is comprised from signals from the data signals or different signals, and it makes the claim indefinite.

Regarding claim 64, the claim is indefinite because no basis can be definitively made for "physically adjacent" outputs.

Claim Objections

12. Claims 1-11, 20-31, and 40-65 are objected to because of the following informalities:

Regarding claim 1, in line 1, "clock synchronization circuit" should be replaced by –clock synchronization circuit (CSC)--, and, in line 2, "current data signals and future data signals" should be replaced by –current data signals and respective future data signals—to properly embody the invention.

Regarding claim 2, in lines 3 and 5, "current and future" should be replaced by –current and respective future—in each case to properly embody the invention.

Regarding claim 4, in line 2, "the delayed clock signal" should be replaced by –the phase shifted clock signal–.

Regarding claim 5, in lines 2-3, "the read data" and "the output data" are lacking antecedent basis, and, in lines 6 and 8, "the phase shift control signals" should be replaced by –the plurality of phase shift control signals—

Regarding claim 6, "read data" and "output data" signals are lacking antecedent basis in the claim, and in lines 3-4, "a corresponding phase shift control signal" should be replaced by –a corresponding one of the plurality of phase shift control signals–.

Regarding claim 7, in line 5 and lines 6-7, "the phase shift control signal" should be replaced by –the respective one of the phase shift control signals—to properly embody the invention, and, in lines 12-13 "the first and second delay elements" are lacking antecedent basis.

Regarding claim 10, in lines 1-2, "each switching circuit" should be replaced by –each of the plurality of switching circuits–, and, in line 6, "delay control signal" should be replaced by –phase shift control signal–.

Regarding claim 21, to properly embody the invention as disclosed in the specification and to make the claim language strictly definite, it is suggested by the Examiner that the following changes are adopted:

> A data output circuit, comprising:
> a plurality of data drivers, each data driver adapted to receive a respective read data signal and being operable to store the respective read data signal in response to a phase shifted clock signal and output the stored respective read data signal as an corresponding output data signal; and
> a clock synchronization circuit adapted to receive an input clock signal and adapted to receive the respective read and corresponding

output data signals, and coupled to the plurality of data drivers, the clock synchronization circuit operable to generate a phase shifted clock signal in response to the input clock signal and apply the phase shifted clock signal to clock the respective read data signals out of the plurality of data drivers as the corresponding output data signals, the phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the respective read data and corresponding output data signals.

Regarding claim 22, in line 4, "is operable to add" is replaced by –is operable to alternatively add–, and, in line 5, "shiftedclock" should be replaced by –shifted clock--.

Regarding claim 25, to properly embody the invention as disclosed in the specification and to make the claim language strictly definite, it is suggested by the Examiner that the following changes are adopted:

A data output circuit, comprising:

a plurality of data drivers, each data driver adapted to receive a respective read data signal and being operable to store the respective read data signal in response to a phase shifted clock signal and output the stored respective read data signal as an corresponding output data signal;

a logic circuit coupled to receive the respective read data and corresponding output data signals, and operable to develop a plurality of phase shift control signals in response to the respective read data and corresponding output data signals; and

a phase shift circuit adapted to receive ~~the~~ an input clock signal and coupled to the logic circuit to receive the plurality of phase shift control signals, and operable to generate the phase shifted clock signal responsive to the input clock signal, the phase shifted clock signal having a phase shift determined by the plurality of phase shift control signals.

Regarding claim 26, in lines 2-3, "a respective read data signal and the corresponding output data signal" should be replaced by –a one of the respective read data and corresponding output data signals–, and, in lines 3-4, "a corresponding phase shift control signal responsive to read data and output data signals" should be replaced by –a corresponding one of the phase shift control signals responsive to the one of the respective read data and corresponding output data signals--.

Regarding claim 27, in line 5, "the phase shift control signal" should be replaced by –the respective one of the phase shift control signals--, in line 6, "a first delay" should be replaced by –a respective first delay–, in lines 6-7, "the phase shift control signal" should be replaced by –the respective one of the phase shift control signals--, and, in line 14, "the delayed clock signal" should be replaced by –the phase shifted clock signal--.

Regarding claim 30, in line 2, "first capacitor between" should be replaced by –first capacitor collectively coupled between—, in line 4, "second capacitor between" should be replaced by –second capacitor collectively coupled between—, and, in line 6, "delay control signal" should be replaced by –phase shift control signal--.

Regarding claim 40, in line 11, "current data signals and future data signals" should be replaced by –current data signals and respective future data signals—to properly embody the invention.

Regarding claim 42, the claim is objected to for the same reasons as applied to claim 40 above.

Regarding claim 44, in line 3, "a first logic state of each logic signal" should be replaced by –a respective first logic state of each of the data signals--, in line 4, "a second logic state of each data signal" should be replaced by –a respective second logic state of each of the data signals--, in line 5, "detected first and second" should be replaced by –detected respective first and second--.

Regarding claim 45, in lines 1-2, "the first logic state of each data signal" should be replaced by –the respective first logic state of each of the data signals--, and, in line

2, "the second logic state of each data signal" should be replaced by –the respective second logic state of each of the dart signals--.

Regarding claim 46, in line 2, "detected first and second logic" should be replaced by –detected respective first and second logic--, in line 3, "each pair of detected first and second logic" should be replaced by –each corresponding pair of respective first and second logic--, in line 4, "detected first and second logic" should be replaced by –detected respective first and second logic--, in line 5, "each pair of detected first and second logic" should be replaced by –each corresponding pair of respective first and second logic--, and, in line 6, "detected first and second logic" should be replaced by --detected respective first and second logic--.

Regarding claim 48, in line 3, "a current logic state of each data signal" should be replaced by --a respective current logic state of each of the data signals--, in line 4, "a future logic state of each data signal" should be replaced by –a respective future logic state of each of the data signals--, and, in line 6, "detected first and second logic states of each data signal" should be replaced by –detected respective first and second logic states for each of the data signals--.

Regarding claim 48, in line 1, "an output" should be replaced by –the output--, in line 2, "each pair of current" should be replaced by –each corresponding pair of respective current ", in line 3, "detected current" should be replaced by –detected respective current--, and, in line 4, "each pair of current" should be replaced by –each corresponding pair of respective current--.

Regarding claim 57, in line 3, "a first logic state of each data signal" should be replaced by –a respective first logic state of each of the data signals--, in line 4, "a second logic state of each data signal" should be replaced by –a respective second logic state of each data signal--, in line 5, "for each data signal" should be replaced by –for each of the data signals--, and, in line 6, "detected first and second" should be replaced by –detected respective first and second--.

Regarding claim 58, in lines 1-2, "the first logic state of each data signal" should be replaced by –the respective first logic state of each of the data signals--, and, in line 2, "the second logic state of each data signal" should be replaced by –the respective second logic state of each of the data signals--.

Regarding claim 59, in line 1, "an output delay" should be replaced by –a respective output delay--, in line 2, "detected first and second" should be replaced by –detected respective first and second--, and, in line 3, "each data signal" should be replaced by –each of the data signals--.

Regarding claim 63, in line 3, "a future logic state of each data signal" should be replaced by –a respective future logic state of each of the data signals--, in line 4, "each data signal" should be replaced by –each of the data signals--, in line 5, "the current ... logic states" is lacking antecedent basis, in line 7, "for each data signal" should be replaced by –for the data signals--, in line 8, "first and second logic states" has no antecedent basis.

Appropriate correction is required.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art of record cited on the accompanying PTO-892 is cited to further show the state of the art with respect to output transition synchronization.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. *The Applicant is invited to contact the examiner if any clarification of the above claim objections and rejections should be made to expedite the prosecution.* The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
May 18, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER